REMARKS

Claims 1-20 are pending and stand rejected. Claim 1 is amended to clarify the subject matter of the invention. All pending claims, as amended, are believed to be allowable over the references cited by the Examiner as discussed below. Accordingly, a Notice of Allowance for the present application is respectfully requested.

Rejection Under 35 U.S.C. §102(b)

Claims 1, 4-7, 9-11, and 13-29 were rejected under 35 U.S.C. §102(b) as being anticipated by Gaddis.

Independent claim 1, as amended, recites an ATM-Ethernet network system that generally includes an ATM processor, an Ethernet network processor, and an ATM-Ethernet processor. The ATM-Ethernet processor includes a packet buffer pointer ring for managing traffic from the Ethernet network processor to the ATM processor and contains ATM processor packet buffer pointers each including a memory address in a packet buffer of the ATM processor. The ATM-Ethernet processor also includes a packet descriptor ring and a data buffer for managing traffic from the ATM processor to the Ethernet network processor, the packet descriptor ring being configured to contain packet descriptors each including an ATM-Ethernet packet buffer memory address in the data buffer.

Independent claim 10 recites a method for data communication that generally includes receiving a packet from a network processor by an ATM-Ethernet processor for transmission to an ATM processor, fetching a packet buffer pointer from a packet buffer pointer ring of the ATM-Ethernet processor, the packet buffer pointer including a memory address pointing to a packet buffer memory location in a data buffer memory of the ATM processor, and transmitting the fetched packet buffer pointer and the received packet to the ATM processor.

Independent claim 16 recites a method for data communication that generally includes receiving a packet from an ATM processor by an ATM-Ethernet processor for transmission to a network processor, storing the packet in a data buffer of the ATM-Ethernet processor, storing a packet descriptor for the packet in a packet descriptor ring of the ATM-Ethernet processor, the packet descriptor including a pointer to a memory location in the data buffer to which the packet is stored, and analyzing the packet descriptor for error. If an error is detected, then the method generally includes dropping the packet descriptor and reporting the error to the ATM processor.

On the other hand, if no error is detected, then the method generally includes fetching the packet from the data buffer of the ATM-Ethernet processor and transmitting the packet to the network processor.

Gaddis discloses a system in which the Ethernet-to-ATM traffic as well as the ATM-to-Ethernet traffic share a dual-ported shared memory 24. The receive buffer descriptors (for the Ethernet-to-ATM path) and the transmit buffer descriptors (for the ATM-to-Ethernet path) contain memory addresses in the same dual-ported shared memory 24. (See FIG. 3 and col. 5, line 54-col. 6, line 17).

In contrast, independent claim 1 as amended, for example, recites that the ATM-Ethernet processor includes a packet buffer pointer ring containing ATM processor packet buffer pointers each including a memory address in *a packet buffer of the ATM processor* as well as a packet descriptor ring containing packet descriptors each including an ATM-Ethernet packet buffer memory address *in the data buffer.*

Similarly, independent claim 10 also recites that the ATM-Ethernet processor includes a packet buffer pointer ring containing a packet buffer pointer that includes a memory address pointing to a packet buffer memory location in a *data buffer memory of the ATM processor.*

Furthermore, in each of independent claims 1, 10, and 16, the packet buffer pointer ring and/or the packet descriptor ring are stored in a configuration of a ring which allows each to be scalable (see, for example, specification at paragraph [0019]).

Withdrawal of the rejection of claims independent claim 1 and 10 as well as claims dependent therefrom under 35 U.S.C. §102(e) is respectfully requested.

Rejections Under 35 U.S.C. §103

Claims 2 and 12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gaddis in view of Vogel. Claim 3 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Gaddis in view. Claim 8 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Gaddis in view of Yoaz. Claim 20 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Gaddis in view of Rozario.

However, claims 2, 3, 8, 12, and 20 are believed to be allowable at least because the independent claims from which they variously depend are believed to be allowable as discussed

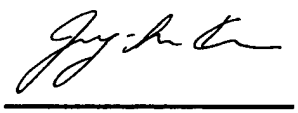
above. Withdrawal of the rejection of these claims under 35 U.S.C. §103(a) is respectfully requested.

CONCLUSION

Applicants believe that all pending claims are allowable and respectfully request a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

In the unlikely event that the transmittal letter accompanying this document is separated from this document and the Patent Office determines that an Extension of Time under 37 CFR 1.136 and/or any other relief is required, Applicant hereby petitions for any required relief including Extensions of Time and/or any other relief and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. **50-1217** (Order No. **INTCP004**).

Respectfully submitted,



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